REMARKS

Claims 1-11 are pending in the application. By this Amendment, a substitute Title and a substitute Abstract are provided, the specification is amended, claims 1 and 4 are amended, and new claims 5-11 are added.

The amendments to the application are fully supported by the application as originally filed, and do not add new matter to the application. With respect to the claim amendments and additions, see for example the originally filed specification at page 9, line 19 to page 10, line 4.

In the Office Action, the Examiner objects to the title as not being descriptive. Applicant respectfully submits that the substitute Title provided herewith obviates this objection.

In the Office Action, the Examiner objects to the Abstract. Applicant respectfully submits that the substitute Abstract filed herewith obviates this objection. Withdrawal of the objection is respectfully requested.

In the Office Action, the Examiner objects to the disclosure on grounds it contains various informalities. Applicant respectfully submits that the amendments to the specification provided herewith obviate this objection. Withdrawal of the objection is respectfully requested.

In the Office Action, the Examiner rejects claims 1-4 under 35 U.S.C. § 102(b) over U.S. Patent No. 3,624,501 to Joseph (Joseph). This rejection is respectfully traversed.

Joseph discloses an integrating circuit wherein a large capacitor switched out of a parallel connection with a smaller capacitor, thus reducing the integrating capacitance in

order to shorten the time constant and thereby allow an easy and rapid initial setting of a rate meter. See for example Joseph at C1/L5-15, C1/L21-23 and C1/L63-64.

Joseph fails to disclose or suggest means for selectively switching said at least one additional charge well in parallel with said first charge well to vary the integration time of said moving charges, *based on a brightness of a target*, as recited in claim 1. Joseph likewise fails to disclose or suggest selectively varying an integration capacitance to vary the integration time of moving charges, *based on a brightness of a target*, as recited in claim 4.

Joseph also fails to disclose or suggest that the means for selectively switching, switches *based on a range to the target*, as recited in claim 5. Joseph likewise fails to disclose or suggest selectively varying the integration capacitance to vary the integration time of the moving charges *based on a range to the target*, as recited in claim 6.

Joseph also fails to disclose or suggest means for selectively switching the at least one additional charge well in parallel with the first charge well to vary the integration time of the moving charges, *based on a rate at which the moving charges fill the first charge well*, as recited in claim 7. Joseph likewise fails to disclose or suggest selectively varying said integration capacitance to vary the integration time of said moving charges, *based on a rate at which the moving charges fill the first charge well*, as recited in claim 10.

Joseph also fails to disclose or suggest that the means for selectively switching, switches *based on a remaining capacity of the first charge well*, as recited in claim 8. Joseph likewise fails to disclose or suggest selectively varying said integration capacitance to vary

the integration time of said moving charges *based on a remaining capacity of the first charge well*, as recited in claim 11.

For at least the above reasons, Applicant respectfully submits that Joseph fails to disclose or suggest the claimed invention. Withdrawal of the rejection of claims 1-4 under 35 U.S.C. § 102(b) over Joseph is respectfully requested.

Applicant respectfully submits that the application is in condition for allowance. Favorable consideration on the merits and prompt allowance are respectfully requested. In the event any questions arise regarding this communication or the application in general, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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Date: 16 May 2002

Attachment to Amendment dated 15 May 2002

Marked-up replacement paragraphs

First Paragraph on page 1

The present application is related to Application [Serial] No. [_____] 09/666,847 (Attorney Docket No. 017750-410), entitled "Three Color Quantum Well Focal Plane Arrays", Application [Serial] No. [_____] 09/666,828 (Attorney Docket No. 017750-442), entitled "Programmable Hyper-Spectral Infrared Focal Plane Array," Application [Serial] No.[_____] 09/666,297 (Attorney Docket No. 017750-444), entitled "Remote Temperature Sensing Long Wavelength Modulated Focal Plane Array, Application [Serial] No. [_____] 09/665,959 (Attorney Docket No. 017750-443), entitled "Clutter Discriminating Focal Plane Array," and Application [Serial] No. [_____] 09/666,296 (Attorney Docket No. 017750-447), entitled "Large Dynamic Range Focal Plane Array," all filed on even data herewith. The disclosures of the above identified Patent Applications are herein incorporated by reference.

Attachment to Amendment dated 15 May 2002

Marked-up replacement paragraphs

Paragraph beginning on page 9, line 19 and ending on page 10, line 4

A third advantageous function performed by the exemplary read out circuit of Figure 2 is the improvement of the gain and dynamic range of the read out circuit through the use of two charge wells. At long ranges with faint targets, the number of volts per electron becomes a significant factor and signal to noise ratios thus become critical. As a hot target gets closer, the need changes from the need for maximizing the noise to avoiding saturation due to the very large number of target electrons rapidly filling the charge well. The exemplary read out circuit of Fig. 2 solves this problem by augmenting the integration time through a change in the charge well capacitance. This is [illustrated in Figure 4 by the use of] done via the two charge well capacitances C_{w1} **200** and C_{w2} **205**. Application of a gain switching voltage GN **240** switches in the smaller charge well capacitance C_{w2} **205** to add another twenty decibels of dynamic range to the system's performance. A high total dynamic range performance of 128 decibels can thus be realized (68 dB small well, 40 dB integration time modulation, and 20 dB well change).

Attachment to Amendment dated 15 May 2002

Marked-up replacement paragraphs

Paragraph beginning on page 10, line 17 and ending on page 11, line 7

Another advantageous function of the read out circuit is the elimination of electronic cross coupling. Electronic cross coupling can be avoided by having each color of the detector use its own time division multiplexer and output port. Since most electronic cross talk in time division multiplexers is capacitive, use of very low driving point impedance in the line and column process is important in holding down the temporal-spectral cross talk. This is particularly imperative in high speed applications with wide dynamic range requirements. These characteristics can be achieved[, as shown in Figure 4,] through the use of the dual FET M7 **250** and push/pull operational amplifier **255**. The dual FETs **250** open or close based on time division multiplexing voltages LINE **260** or COLUMN **265**. The LINE **260** voltage is used to access a line of cells in the focal plane array and the COLUMN **265** voltage accesses a column of cells in the focal plane array. The push/pull operational amplifier **255** additionally sets the voltage gain of the output circuit to the following relationship:

$$\frac{V_o}{V_i} = \frac{R_F}{R_I(1+\frac{R_F}{R_I})}$$

Eqn. (6)

The driving point impedance is further set by the resistor R_O **270**.

Attachment to Amendment dated 15 May 2002

Marked-up Claims 1 and 4

1. A circuit for varying the integration time of moving charges from a photodetector comprising:

a first charge well for receiving moving charges from a photodetector;

at least one additional charge well; and

means for selectively switching said at least one additional charge well in parallel with said first charge well to vary the integration time of said moving charges, based on a brightness of a target.

2. The circuit of claim 1, wherein said first charge well comprises a capacitor.

3. The circuit of claim 1, wherein said at least one additional charge well comprises a capacitor.

4. A method of varying the integration time of moving charges from a photodetector comprising the steps of:

supplying moving charges from a photodetector to an integration capacitance; and

selectively varying said integration capacitance to vary the integration time of said moving charges, based on a brightness of a target.